ABSTRACT

A clock synthesizing circuit for generating clock signals for driving a pixel-based image sensor includes a pixel rate generator that generates a master clock having a master clock frequency corresponding generally to a readout rate of the image sensor, a frequency locked loop that receives the master clock and generates a high frequency clock operating at a multiple of the master clock frequency, and a clock generation circuit that utilizes the high frequency clock to generate a plurality of low frequency clock signals for driving the image sensor. The frequency locked loop may be either a phase locked loop or a delay locked loop, and the clock generation circuit would utilize the edge transitions of the high frequency clock to generate the low frequency clock signals for driving the image sensor.